

Telephone Line Interface and Speakerphone Circuit

AES2523, AES2524, AES2524B

PRELIMINARY DATA SHEET

Key Features

- Line/Speakerphone circuit on a 28-pin CMOS-IC, simple inventory: same die for AES2523/24 and AES2523/24B
- Serial I/F on AES2523, parallel I/F on AES2524
- Enhanced voice switching
- Background noise monitoring
- Tx- and Rx-gain programmable on AES2523 only
- Digital volume control of Rx signals on AES2523 only
- DC characteristic programmable on AES2523 only
- Dual softclipping in handset mode
- Dual softclipping in handsfree mode
- Loudspeaker amplifier for loudhearing and handsfree
- Supply voltage generation for external circuitry
- Automatic line loss compensation on AES2523 / 24B only
- Real and complex impedance selectable by external components
- Side tone adaptation selectable by external components
- Unique EMC performance
- Operating range from 15mA to 100mA (down to 5mA with reduced performance)
- Few external components

General Description

AES2523/24 is a CMOS integrated circuit that incorporates DC and AC line adaptation (DC-mask and synthesized AC-impedance of 1000Ω) as well as a speech circuit with softclipping, line loss compensation and Rx-volume control for handset and handsfree operation. It shall act as an a/b-line powered device, which is controlled by a CPU via a serial interface on AES2523 or a standard dialler via a parallel interface on AES2524 and AES2524B.

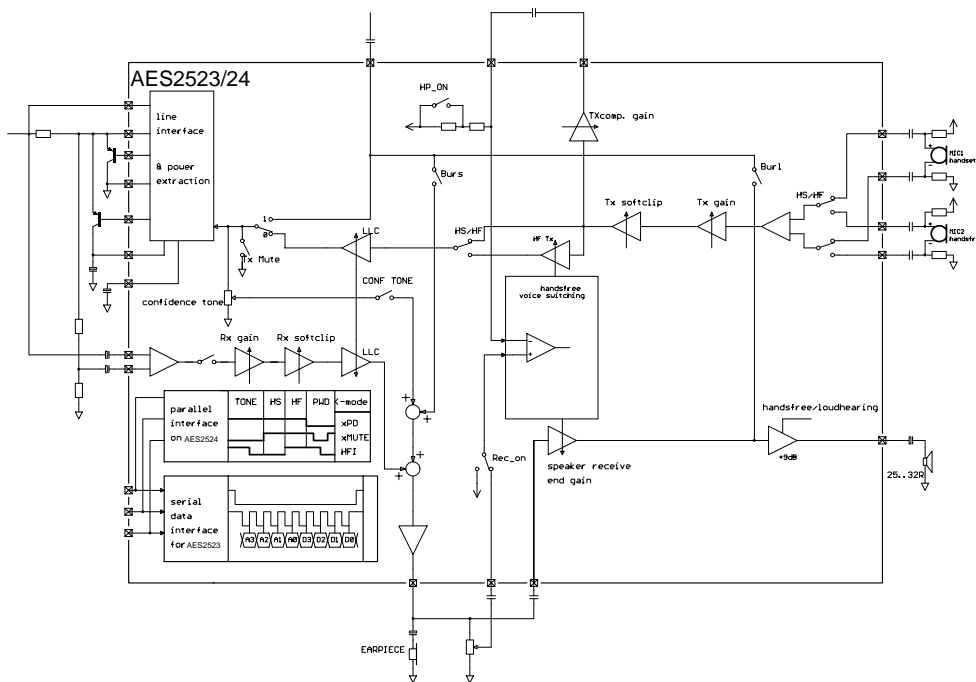
Applications

Enhanced handsfree feature phones with CallerID and extended displays. The AES2524 and AES2524B are developed to interface with common Taiwanese diallers.

Package

Available in 28-pin SOIC or die

Block Diagram

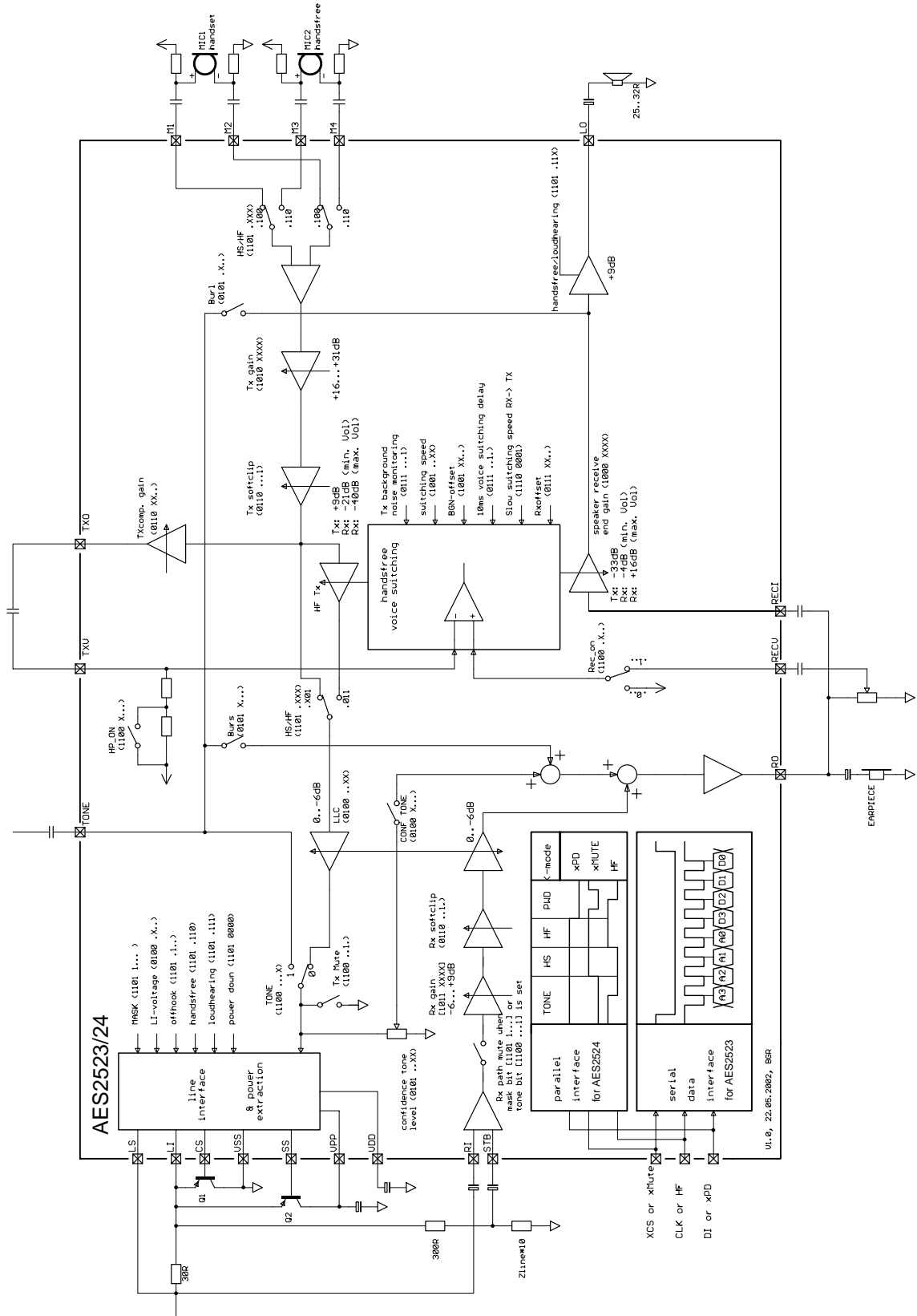


Pin description

Pin #	Symbol	Function
15	LS	Line Current Sense Input Analog input for sensing the line current
12	LI	Line Input Analog input used for power extraction and line current sensing
13	RI	Receive Input Analog input for ac-separated receive signal
9	STB	Side Tone Balance Input Analog input for side tone cancellation network
10	CS	Current Shunt Control Output N-channel open drain output to control the external high power shunt transistor for synthesizing AC- and DC-impedance, modulation of line voltage and shorting the line during make periods of pulse dialing
16	CI	Complex Impedance Input Analog input pin for the capacitor to program a complex impedance
14	SS	Supply Source Control Output N-channel open drain output to control the external high power source transistor for supplying (Vpp) the loudspeaker amplifier in off-hook loudspeaking/handsfree mode
11	VSS	Voltage Source Source Negative Analog Power Supply
18	VDD	Voltage Drain Drain Positive Analog Power Supply
19	AGND	Analog Ground Special ground for the internal amplifiers
8	M1	Microphone Input 1 Differential input for the handset microphone (electret)
6	M2	Microphone Input 2 Differential input for the handset microphone (electret)
7	M3	Microphone Input 3 Differential input for the handsfree microphone (electret)
5	M4	Microphone Input 4 Differential input for the handsfree microphone (electret)
17	RO	Receive Output to Handset Output for driving a dynamic earpiece with an impedance from 150Ω to 300Ω

Pin #	Symbol	Function
25	xCS /xMUTE	Chip Select on AES2523 Chip select input of the serial interface. Internal pull-up resistor (100kOhm) Mute transmit-, receive- path and activate tone path on AES2524 and AES2524B
26	DI /xPD	Data Input on AES2523 Data input of the serial interface. Internal pull-up resistor (100kOhm) Power down mode for AES2524 and AES2524B (On-hook)
27	CLK /HFE	Clock on AES2523 Clock input of the serial interface. Internal pull-up resistor (100kOhm) Handsfree mode operation on AES2524 and AES2524B
23	LO	Loudspeaker Output. Output pin is for a 25Ω loudspeaker
2	FT1	Analog input pin for connecting a capacitor for offset cancellation.
3	TXO	Analog output of the transmit signal
4	TXV	Analog input for the transmit signal in the voice switching path
1	CBN	Analog input pin for connecting a capacitor for background noise monitoring.
20	RECI	Analog input for the handsfree receive path. Should be connected to RO via coupling capacitor.
21	RECV	Analog input for receive voice switching path.
24	VSSA	Power supply pin for LO output amplifier.
22	VPP	Power supply pin for LO output amplifier.
28	TONEIN	Analog input for DTMF-signals.

Detailed Block Diagram



Functional Description

DC conditions

The normal operating mode is from 15mA to 100mA. An operating mode with reduced performance is from 5mA to 15mA. In the line hold range from 0mA to 5mA the device is in a power down mode.

The DC characteristic is determined by the voltage at LI-pin and a 30Ω resistor between LI- and LS-pin. It can be calculated by the following equation: $V_{LS} = V_{LI} + I_{Line} \cdot 30\Omega$. V_{LI} can be programmed to be 3.5V or 4.5V.

2/4 wire conversion

AES2523/24 has built in two Wheatstone bridges with one common ground. This provides a maximum of independence of AC-impedance and side tone from each other. One can adapt side tone without changing the AC-impedance.

AC-impedance

The AC-impedance of AES2523/24 is set to t.m. 100Ω. With the external capacitor at CI-pin it can be programmed complex. With an external resistor of approx. 1.5kΩ connected to the LS-pin it can be programmed to 600Ω.

Side Tone

A good side tone cancellation can be achieved by using the following equation:

$$Z_{BAL}/Z_{LINE} = 10$$

Transmit path

The gain of the M1/M2 → LS is set to +37dB. This gain can be changed by programming on AES2523 from +30dB to +45dB in 1dB steps (Register *Txgain*), on AES2524 / 24B it is set to +37dB per default. The input is differential with an impedance of 10kΩ. The soft clip circuit limits the output voltage at LS to 2Vp. There is LLC for this path.

The gain of the M3/M4 → LS is set to +46dB.

This gain can be changed by programming from +39dB to +54dB in 1dB steps on AES2523. The input is differential with an impedance of 10kΩ. The soft clip circuit limits the output voltage at LS to 2Vp. There is no LLC for this path.

Receive path

The gain of the LS → RO receive path is set to +7.5dB.

This gain can be changed by programming from -7.5dB to +7.5dB in 1dB steps (Register *Rxgain*). The receive input is the differential signal of RI and STB. The soft clip circuit limits the output voltage at RO to 1Vp. It prevents harsh distortion and acoustic shock. There is LLC for this path.

The gain of the LS → LO receive path is set to +32dB.

This gain can be changed by programming from +19dB to -34dB in 1dB steps. The user can also change the gain via Register *Handsfree receive end gain* (See section "Handsfree"). The receive input is the differential signal of RI and STB. The soft clip circuit limits the output voltage at LO to 1.1Vp. It prevents harsh distortion and acoustic shock. There is optional LLC for this path.

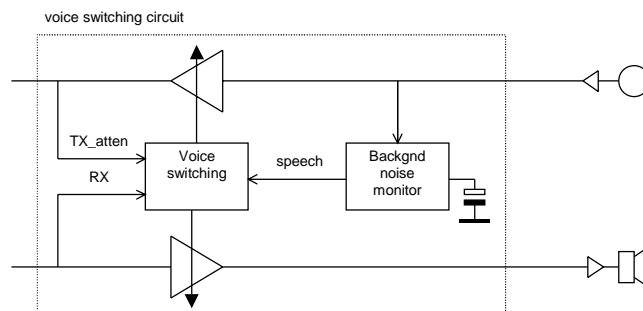
Line Loss Compensation (AES2523, AES2524B)

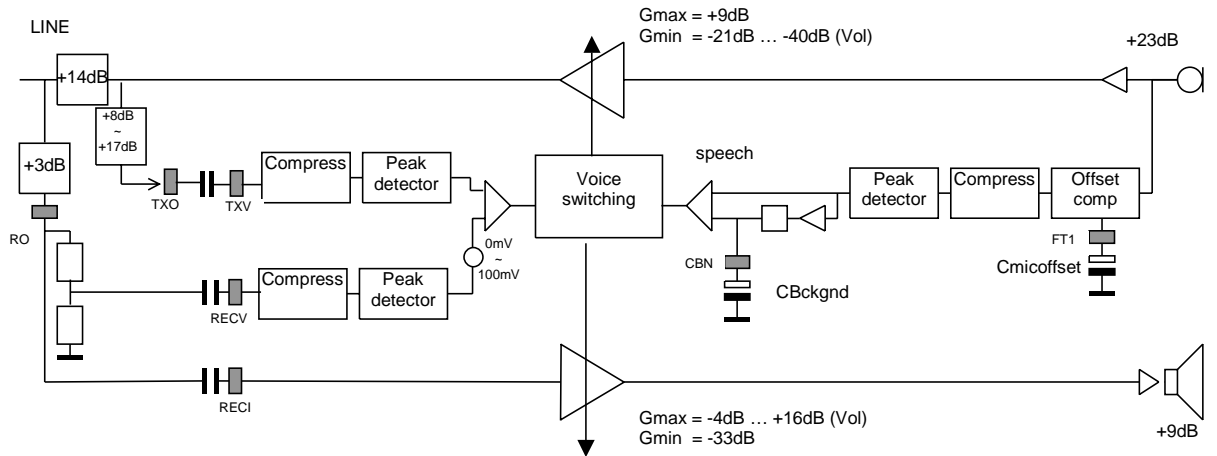
- programmable on AES2523
- not activated at AES2524
- permanently activated at AES2524B

When it is activated, the transmit and receive gains for both I/O's are decreased by 6dB at line currents from 20mA to 50mA or from 45mA to 75mA.

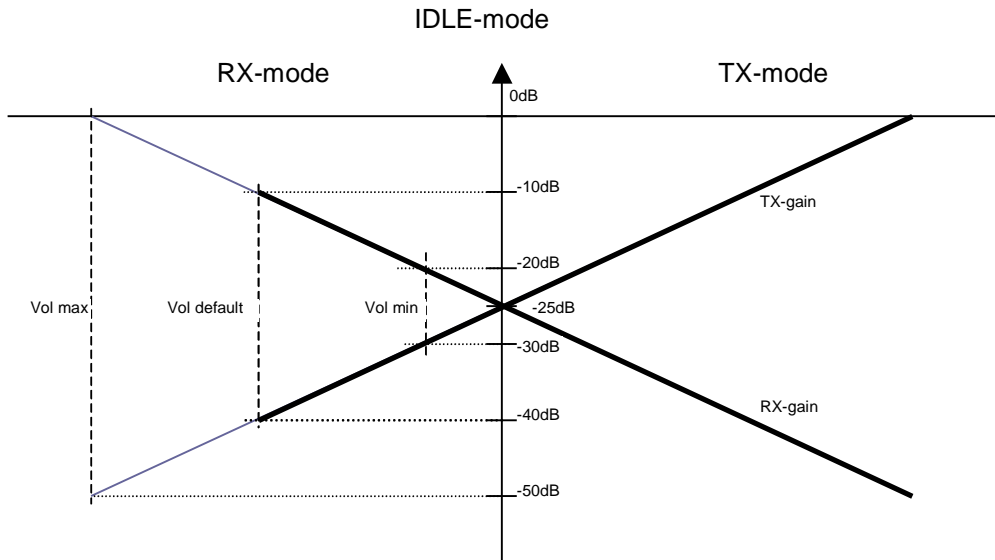
Handsfree

The handsfree function allows voice communication without using the handset (full 2-way speaker phone). Two voice controlled attenuators prevent acoustic coupling between the loudspeaker and the microphone. The voice switching circuit has three states, namely idle, transmit or receive. In receive mode the attenuation of the receive path and the transmit path can be controlled by Register *Handsfree receive end gain* between 0dB and -20dB. The following table shows how voice switching is controlled





	Speech	Mode	Rx-gain	Tx-gain	Remark
Rx > Tx_atten	X	Receive	0db to -20dB	-50dB to -30dB	adjustable with VOL-setting
Tx_atten > Rx	NO	Idle	-25	-25	middle position
Tx_atten > Rx	YES	Transmit	-50dB	0dB	independent of VOL-setting



Typical Characteristics of Line Loss Compensation (AES2523, AES2524B only)

The line-loss-compensation is programmable at the AES2523, not activated at the AES2524 and LLC high (45mA-75mA) activated at the AES2524B.

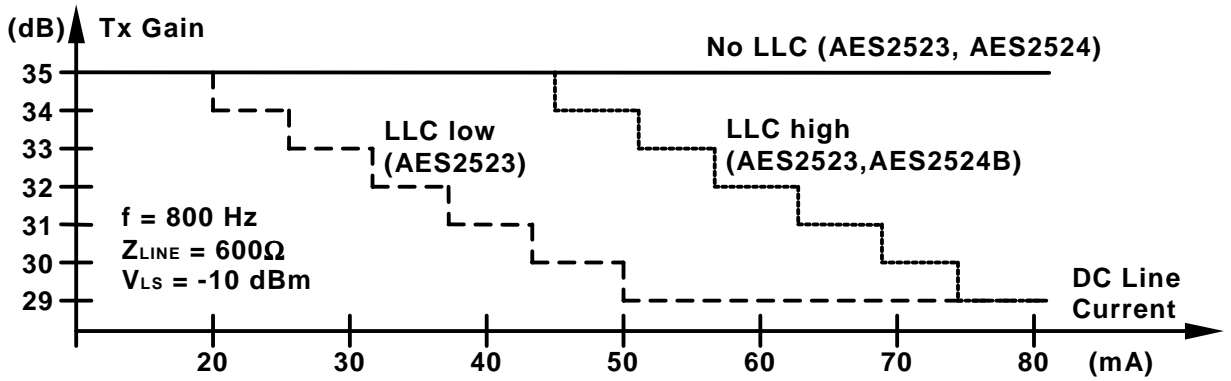


Figure 1 Typical Tx Gain Characteristics Line Loss Compensation

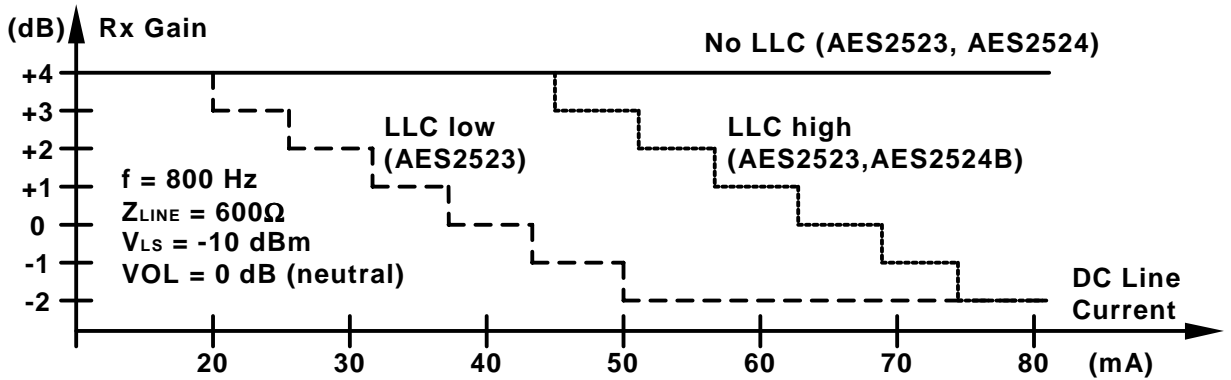


Figure 2 Typical Rx Gain Characteristics Line Loss Compensation

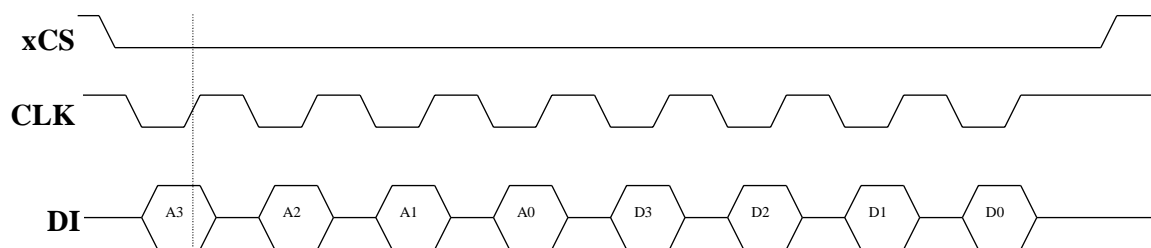
Serial Interface on AES2523

Registers

The settings of the AES2523 are stored in 16 registers. Each register has 4 bit data width.

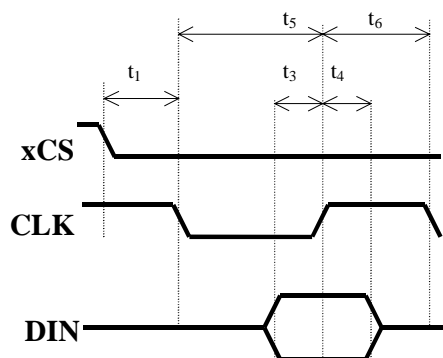
Timing

The data format for writing to a register has the following form:



Note: The pins xCS,CLK,DI have internal pull-up resistors.

Parameter	Symbol	MIN	TYP	MAX
CLK Pulse width HIGH	T6	100ns		
CLK Pulse width LOW	T5	100ns		
xCS to first falling CLK-edge setup time	T1	50ns		
DIN to CLK setup time	T3	50ns		
DIN to CLK hold time	T4	50ns		



Serial interface Registers

The following table shows the content of the 16 control registers.

Address	Data	Control registers AES2523	Default value after reset	
A A A A	D D D D		for AES2523, AES2524HF	AES2524 LH bond option
3 2 1 0	3 2 1 0			
0 0 0 0	Nop		na	na
0 0 0 1			na	na
0 0 1 0			na	na
0 0 1 1			na	na
0 1 0 0	x x x x	Conf-Tone: 0... No Conf Tone 1... Conf Tone LIV: Voltage at pin LI 0...3.5V, 1...4.5V LLC1 LLC0: Line loss compensation setting 0 0 20mA-50mA 0 1 NO Line loss compensation 1 0 45-75mA 1 1 NO Line loss compensation	0111	0111
0 1 0 1		BURS: Analog tone at RO 0...OFF, 1...ON BURL: Analog tone at LS 0...OFF, 1...ON CTL CTO: @RO @LS 0 0 -36dB -15dB TONE-confidence level 0 1 -30dB -9dB rel. to pin LS 1 0 -24dB -3dB 1 1 -18dB +3dB	0001	0001
0 1 1 0	x x x x	Softclip-settings, Tx_comp_gain settings Bit1 Bit0 :Tx_comp_gain 0 0 +8dB 0 1 +11dB 1 0 +14dB 1 1 +17dB SOFTRX: Softclip RX 0...OFF, 1...ON SOFTTX: Softclip TX 0...OFF, 1...ON	1000	1000
0 1 1 1		Bit1 Bit0: Rx-offset setting 0 0 0mV 0 1 12mV 1 0 40mV 1 1 100mV Delay_10ms 0... no delay 1... 10ms delay Bnon 0... BGN off 1... BGN on	0101	1100
1 0 0 0	16 gains	Handsfree receive endgain Data RXgain TXgain 0x0 -20dB -30dB Min. receive volume : : 0xF +0dB -50dB Max. receive volume	1111	1011
1 0 0 1	x x x x	off1 off0: BGN-offset 0 0 120mV 0 1 180mV 1 0 240mV 1 1 300mV Hfs1 HF0: Speed of voice switching 0 0 max speed 0 1 1 0 1 1 min speed	0000	1100
1 0 1 0	16 gains	Transmit gain [16], 16 steps, 1dB stepsize Data HS-mode HF-mode 0x0 30dB 39dB : : 0xF 45dB 54dB	0111	0111
1 0 1 1	16 gains	Receive gain [16], 16 steps, 1dB stepsize Data HS-mode HF-mode 0x0 -6dB 19dB : : 0xF +9dB 34dB	1111	1111
1 1 0 0		HP_on : 0... fg=200Hz 1... fg=2000Hz rec_on : 0... Rxcomp=AGND 1... Rxcomp=RECV Mute : 0... No mute 1... Tx-path muted Tone : 0... Tx-signal path 1... Ton in signal path	0100	1000
1 1 0 1	x x x x	Mask, Lh, Hf, Hook Switch Mask: 0... No mask 1... Mask acitivated His HF LH: Hook functions 0 x x Power down 1 0 0 Handset 1 0 1 not allowed 1 1 0 Handsfree 1 1 1 Loudhearing	0100	0101
1 1 1 0	x x x x	slow_rec: fast change to TX, slow change to RX, no IDLE Krat5,Test3,Test2: For factory test only !	0000	0001
1 1 1 1	x x x x	Reset to defaults	na	na

Programming Guidelines for the AES2523

The AES2523 is programmed by means of a serial 8-bit shift register. MSB is clocked in first, LSB last.

The first four bits (7,6,5,4) are the addresses of the registers, the last four bits (3,2,1,0) are the data bits.

Each register has a default setting (see data sheet), which is set after power-up of the chip.

The internal registers are RAM-cells. When the AES2523 loses VDD (as in on-hook state) it also loses the register contents.

It is therefore necessary to re-write the affected registers after each hook event. The register contents cannot be read, they can only be written.

Registers need to be re-written after each power-up and after each hook event (handset / handsfree / on-hook).

It is recommended to always initialize the chip with a "reset to defaults command" (Fx) first and then write the appropriate registers that need to be changed from the default setting.

Alternatively, all registers (4 to 16) may be re-written in a bulk at each power-up and hook event (handset / handsfree / on-hook).

This guarantees safe operation in case of unexpected loss of power during normal operation. Re-writing all registers also eases later software updates, as only register contents need to be changed, but no additional command lines need to be inserted.

Example of a typical power-up sequence

A typical power-up sequence will require the following programming.

- determine the cause of power-up (handset / handsfree mode) and set register D accordingly.
Default = handset mode
- Set the LI voltage to 3.5V or 4.5V (default = 4.5V) and Line Loss Compensation (default = off) in register 4
- Set the Confidence Tone level (e.g. the DTMF level which is audible in the handset) and path in register 5
Default = off
- Set the required Tx and Rx gains in Registers A and B
Default = 37dB Tx gain, 1dB Rx gain

Additional settings in Handsfree mode

Note: change the default settings only if necessary:

- A click-free startup can be achieved by starting up in handset mode (=default) and then switching to handsfree, once the chip has stabilized.
- Change the Tx comparator preamplifier gain in register 6
Default = 14dB
- Change the Receive DC offset and Background noise monitoring in Register 7
default = 0mV offset (higher val. puts more weight on Rx)
switching delay default = on
Background Noise Monitoring = on
- Set the speaker amplifier volume in register 8
Default = 0B
- Set the handsfree voice switching speed and Background Noise monitoring offset in register 9:
default voice switching speed = 1ms/6dB (fastest)
default BGN monitoring offset = 240mV (determines the Tx level required to switch from idle to Transmit)

Additional settings during Flash

During a Flash, the AES2523 should be powered down to avoid discharge of VDD:

Set the MASK bit (bit3 in register D) to 1

After the line current is restored, the MASK bit must be cleared again. Other settings do not need to be re-written, as VDD has not discharged. As a safety margin however, it is recommended to re-write all registers after a flash

Additional settings during line breaks

If a line-break-detection (brief interruption of the line while in off-hook state) is implemented, the same rules apply as for a Flash: set the MASK bit to 1 to avoid discharge of VDD. It is recommended to re-write all registers after a line-break, as a line break may take long enough to discharge VDD, even when the MASK bit was set.

General Rules

The serial interface may be programmed at any time, it does not affect the speech quality, e.g. if a register is overwritten with the same value.

It is also possible to re-write all registers periodically. The register is static, therefore it can be clocked at any speed up to 5MHz.

However, electromagnetic pulses on the clock and data lines may cause unwanted programming of the chip. It is therefore recommended to keep these lines short, filter them by a discrete lowpass filter and reduce the clock speed accordingly.

Parallel Interface on AES2524 and AES2524B

Input Signal on Pin			
xPD	xMute	HF	Mode
0	0	0	Power down
0	0	1	Power down
0	1	0	Power down
0	1	1	Power down
1	0	0	Tone mode
1	0	1	Tone mode
1	1	0	Handset mode
1	1	1	Handsfree mode

Power down mode

For low power consumption the analog part is turned off during activated power down mode. The Power down mode is used during Flash and Pulse dialing and for On-hook operation.

Handset mode

Speech mode is Handset mode (M1-M2, RO active; LO deactivated)

Parameter	AES2524	AES2524B
LI Voltage	4.5V	4.5V
LLC	No LLC	LLC high (45mA to 75mA)
TX-Gain	+37dB	+43dB
RX-Gain	+7.5dB	+7.5dB
Rx-Softclip	Off	On
Tx-Softclip	Off	Off
Tone	Off	Off

Handsfree mode

Speech mode is Handsfree mode (M3-M4, RO active; LO active)

Parameter	AES2524	AES2524B
LI Voltage	4.5V	4.5V
LLC	No LLC	LLC high (45mA to 75mA)
HF TX-Gain	+46dB	+52dB
HF RX-Gain	+34dB	+34dB
Rx-Softclip	Off	On
Tx-Softclip	Off	Off
Tone	Off	Off
BNM	On	On

Tone mode

This mode is used to send DTMF and FSK data to the line.

Speech mode is Tone mode (M1-M2;M3-M4 muted, Rx path muted, RO and LO active)

Parameter	AES2524	AES2524B
LI Voltage	4.5V	4.5V
LLC	No LLC	LLC high (45mA to 75mA)
Tone TX-Gain	+14dB	+14dB
Confidence tone level	-36dB@Ro -15dB@Lo relative to Pin LS	-36dB@Ro -15dB@Lo relative to Pin LS

Loudhearing AES2524 and AES2524B (feature only available as DIE)

Speech mode is Loudhearing (M3-M4, RO active; LO activated).

Loudhearing can be activated via a bond-option (see document "AES2523/24 Delivery as Dice").

Parameter	AES2524	AES2524B
LI Voltage	4.5V	4.5V
LLC	No LLC	LLC high (45mA to 75mA)
TX-Gain	+37dB	+43dB
RX-Gain	+7.5dB	+7.5dB
Tone	Off	Off
Slow_rec	On	On
RECV pin	Deactivated	Deactivated
Highpass	2000kHz (10nF from TXO->TXV)	2000kHz (10nF from TXO->TXV)
Voice switching speed	120ms/6dB	120ms/6dB
RX-Offset	300mV	300mV

Electrical characteristics

Electrical characteristics are measured with the Test Circuit application. Typical mean values will not be tested.

Absolute maximum ratings

Positive Supply Voltage	-0.3V ≤ VDD ≤ 7V
Input Current	+/- 25mA
Input Voltage (LS)	-0.3V ≤ Vin ≤ 12V
Input Voltage (LI, CS)	-0.3V ≤ Vin ≤ 8V
Input Voltage (STB, RI)	-2V ≤ Vin ≤ VDD+0.3V
Digital Input Voltage	-0.3V ≤ Vin ≤ VDD+0.3V
Electrostatic Discharge (HBM 1.5kΩ-100pF)	+/- 1000V
Storage Temperature	-65°C to +125°C

Recommended operating conditions

Supply Voltage (generated internally)	3V ≤ VDD ≤ 5V
Operating Temperature	-25°C to +70°C

DC characteristics

I_{Line}=15mA w/o operation of any additional external circuitry, unless other specified

Symbol	Parameter	Conditions	Min	Type	Max	Units	Test
I _{DDS}	Operating Current	Speech Mode		3	6	mA	Y
I _{DDH}	Operating Current	Handsfree Mode		7	10	mA	Y
V _{LI}	Line Voltage LIVolt=0	15mA<=I _{LINE} <=100mA	3.2	3.5	3.8	V	Y
	Line Voltage LIVolt=1		4.2	4.5	4.8	V	Y
I _{OL}	Output Current, Sink CS,SS	V _{OL} =0.4V		1		mA	N

Transmit characteristics

I_{Line}=15mA f=800Hz, default settings unless other specified

Symbol	Parameter	Conditions	Min	Type	Max	Units	Test
AM1/2TX	Transmit Gain M1/M2 → LS AES2524 AES2524B	Z _{AC(syn)} =1000Ω	35	+36.5	38	dB	Y
			39	+42.5	44	dB	Y
AM3/4TX	Transmit Gain M3/M4 → LS AES2524 AES2524B	Z _{AC(syn)} =1000Ω	43	+45.0	47	dB	Y
			49	+51	53	dB	Y
A _{tone TX}	Transmit Gain Tone → LS	Z _{AC(syn)} =1000Ω	12	+14dB	16	dB	Y
ΔATX	Variation with frequency	f = 500Hz ... 3.4kHz		±0.8		dB	N
AVRM12	Control range M1/M2 → LS	16 steps		-7/+8		dBr	N
AVRM34	Control range M2/M4 → LS	16 steps		-7/+8		dBr	N
THD	Distortion	V _{LS} =0.25V _{RMS}			2	%	Y
VAGC1	Soft Clip Level M1/M2 → LS at LS			2		VP	N
VAGC2	Soft Clip Level M3/M4 → LS at LS			2		VP	N
ASCO	Soft Clip Overdrive M1/M2 - M3/M4			20		dB	N
t _{attack}	Attack time			70		us/6dB	N
t _{decay}	Decay time			100		ms/6dB	N

Symbol	Parameter	Conditions	Min	Type	Max	Units	Test
ZIN-M1/2	Input Impedance M1/M2			10		k Ω	N
ZIN-M3/4	Input Impedance M3/M4			10		k Ω	N
VINmax	Input Voltage Range M1/2 - M3/4	differential		± 1		Vp	N
VNO	Noise Output Voltage LS	TAMP=25°C Handset mode Gain = 36.5dB			-72	dBmp	Y
AMUTE	Mute Attenuation	Mute activated	60			dB	Y

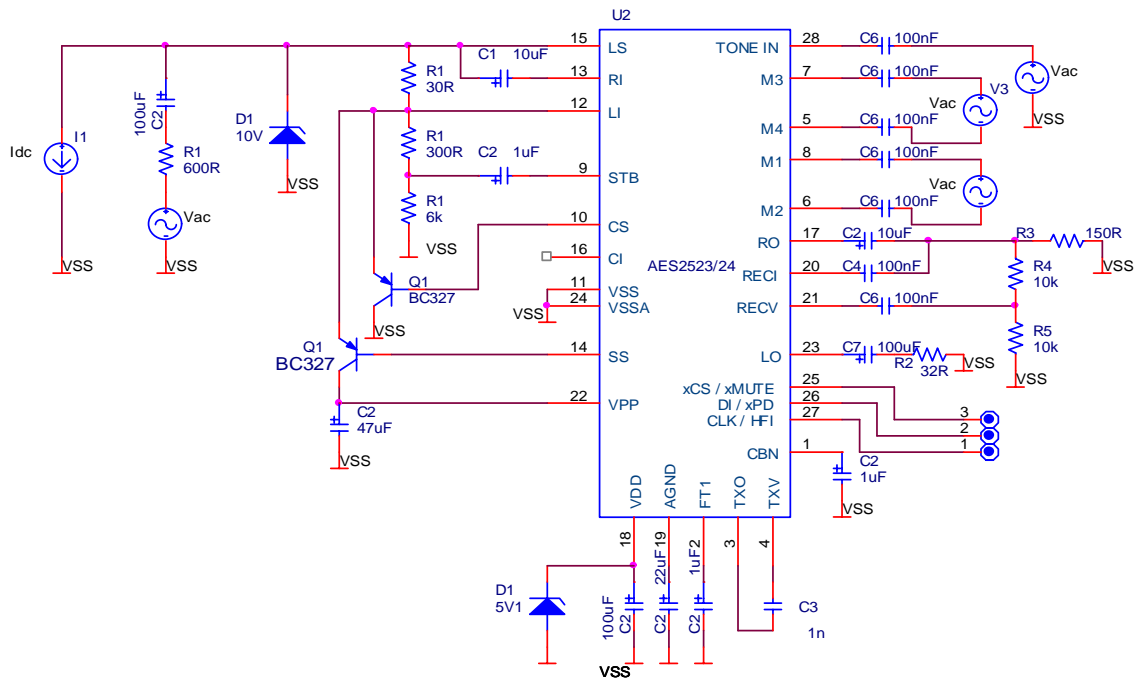
Receive characteristics

I_{Line}=15mA f=800Hz, default settings unless other specified

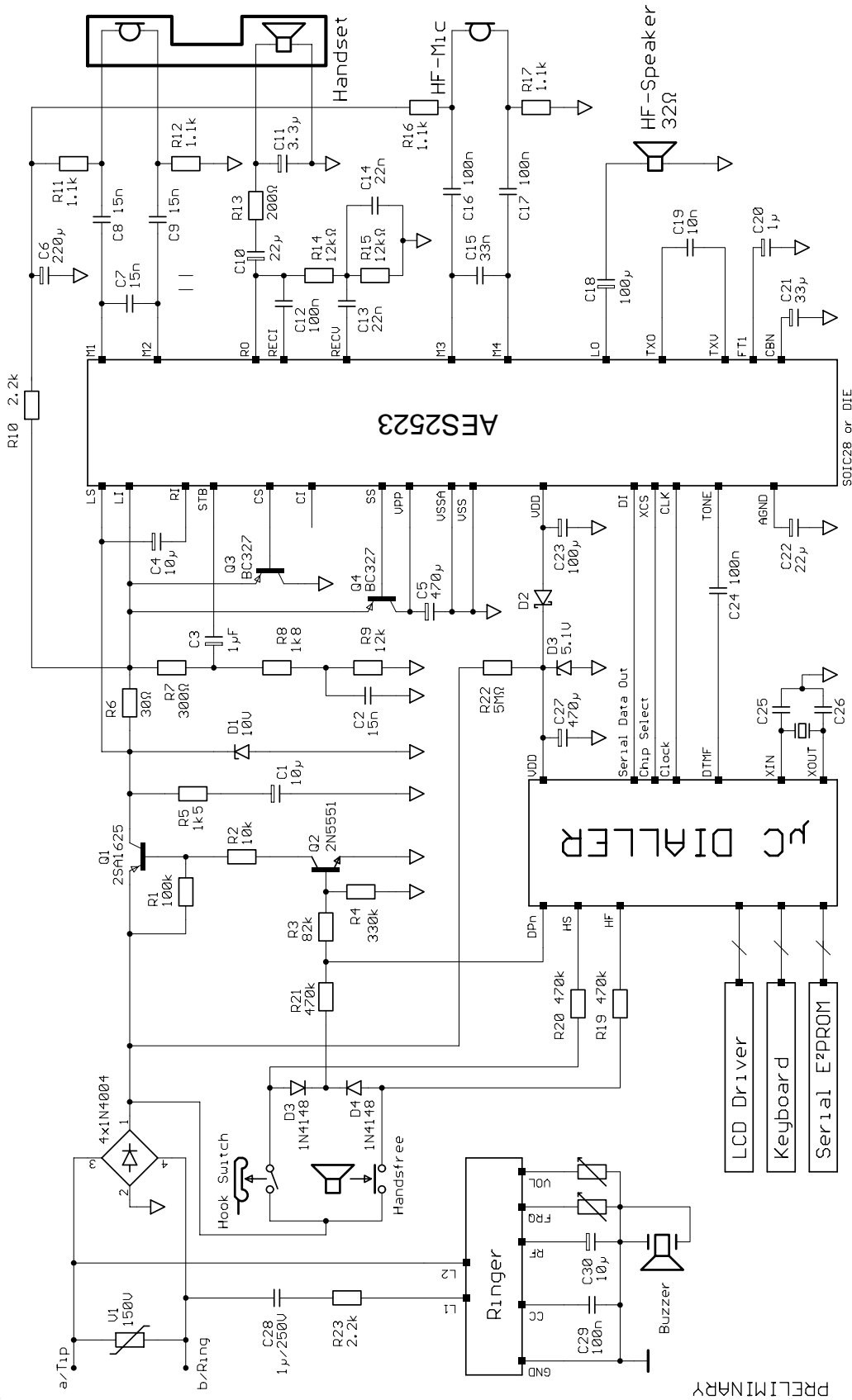
Symbol	Parameter	Conditions	Min	Type	Max	Units	Test
ARO	Receive Gain LS → RO	ZAC(syn)=1000 Ω Vol default	6	+7.5	9	dB	Y
ALO12	Receive Gain LS → LO	ZAC(syn)=1000 Ω Vol maximum	+32.5	+34	+35.5	dB	Y
Δ ARX	Variation with frequency	f=500Hz to 3.4kHz		± 0.8		dB	N
AVRRO	Control range LS → RO	16 steps		-7/+8		dBr	N
AVRLS	Control range LS → LO	16 steps		-7/+8		dBr	N
THDLS	Distortion LO	V _{LS} =0.25V _{RMS}			5	%	Y
THDRO	Distortion RO	V _{LS} =0.25V _{RMS}			2	%	Y
VUFC	Unwanted Freq. Cmp.	f = 200 ... 20kHz			-60	dBm	Y
VAGCRO	Soft Clip Level RO			1		VP	N
VAGCLS	Soft Clip Level LO			1.1		VP	N
ASCLS	Soft Clip Overdrive LO			10		dB	N
Tattack	Attack time			70		us/6dB	N
Tdecay	Decay time			100		ms/6dB	N

Symbol	Parameter	Conditions	Min	Type	Max	Units	Test
VNO	Noise Output Voltage RO	TAMP=25°C Gain = 7.5dB			-68	dBmp	Y
ZIN-RI VINmax	Input Imp. RI Input Voltage Range RI			8 ±2		kΩ Vp	N
ZIN-STB VINmax	Input Imp. STB Input Volt. Range STB			80 ±2		kΩ Vp	N
ST	Side tone	VRI<=0.25VRMS	26			dB	Y
RL ΔZAC/°C	Return Loss Temp. Variation	ZAC(syn)=1000Ω	18	0.5		dB Ω/°C	Y

Test circuit

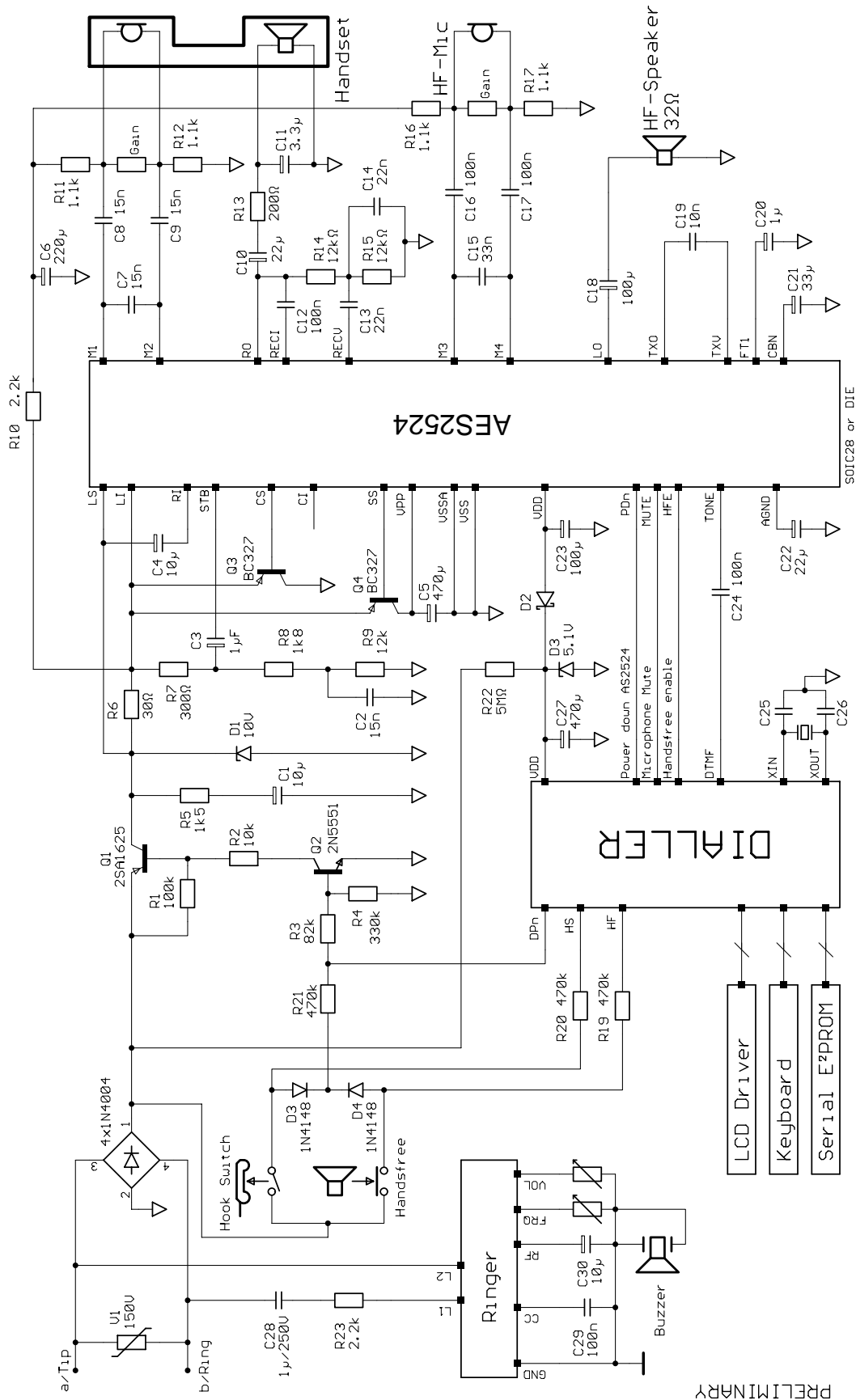


Typical application AES2523



PRELIMINARY

Typical application AES2524 and AES2524B



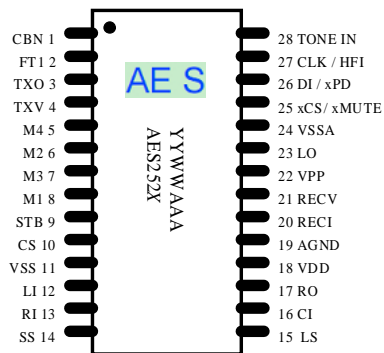
PRELIMINARY

Packaging

28-pin plastic SOIC

For exact mechanical package dimensions please see austriamicrosystemsAG packaging information.

Pin-out, Marking



YY year of production
 WW calendar week of production
 AAA austriamicrosystemsAG assembly ID

X 3 ... AES2523 Version
 4 ... AES2524 Version
 4B .. AES2524B Version

Ordering Information

Number	Package	Description
AES2523 T	SOIC28	plastic surface mounted package – 28 leads
AES2524 T	SOIC28	Plastic surface mounted package – 28 leads
AES2524B T	SOIC28	Plastic surface mounted package – 28 leads
AES2523 F	DOF	Dice-on-Foil
AES2524 F	DOF	Dice-on-Foil
AES2524B F	DOF	Dice-on-Foil

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CERTIFICATE for Telephone IC AES2523/2424B

This is to certify, that the item mentioned above is the original
austriamicrosystems' Telephone IC.

It is packaged and tested by **AE Semiconductor Company** and distributed by
Wisewin Electronics Co (a member of Arthur E Group).

With best regards,

Heribert Hochrinner
World-Wide Marketing Manager for
Wire Line Communication